

## CLAIMS

What is claimed is:

- 1        1.    A memory comprising:  
2                a memory array to store data;  
3                a first pointer coupled to the memory array to  
4                address memory locations therein;  
5                a pointer memory coupled to the first pointer, the  
6                pointer memory to save one or more prior first pointer  
7                values of the first pointer; and  
8                control logic coupled to the pointer memory, the  
9                control logic to restore one of the one or more prior  
10               first pointer values to the first pointer in response to  
11               branch information.
  
- 1        2.    The memory of claim 1, wherein  
2                the first pointer is a pop pointer to read data out  
3                from the memory array,  
4                and  
5                the memory further comprises,  
6                a push pointer to write data into the memory  
7                array.
  
- 1        3.    The memory of claim 1, wherein

2           the branch information includes a branch flag to  
3           indicate a condition that requires the restoration of the  
4           one prior first pointer value to the first pointer.

1           4.    The memory of claim 1, wherein  
2                   the branch information is to be received from a  
3           processor capable of speculatively issuing requests to  
4           read data from the memory array.

1           5.    The memory of claim 1, wherein  
2                   the pointer memory saves a plurality of prior first  
3           pointer values as a history of first pointer values.

1           6.    The memory of claim 2, further comprising:  
2                   status logic coupled to the pop pointer and the push  
3           pointer to monitor a pop pointer value of the pop pointer  
4           and a push pointer value of the push pointer to provide  
5           an indication of an amount of data stored in the memory  
6           array.

1           7.    The memory of claim 6, wherein  
2                   the status logic to generate a high status flag in  
3           response to an amount of data stored in the memory array  
4           being greater than or equal to a high threshold level,  
5           and less than or equal to a maximum utilization level.

1           8.    The memory of claim 7, wherein

2           the status logic to further generate a low status  
3           flag in response to an amount of data stored in the  
4           memory array being less than or equal to a low threshold  
5           level and greater than or equal to an empty threshold  
6           level.

1           9.    The memory of claim 7, wherein  
2                    the high threshold level is responsive to the lesser  
3           of a maximum branch resolution latency and a low  
4           threshold level.

1           10.   The memory of claim 9, wherein  
2                    the maximum branch resolution latency is a depth of  
3           an instruction pipeline in a processor, the processor to  
4           couple to the first-in first-out memory.

1           11.   The memory of claim 1, wherein  
2                    the branch information includes a branch resolution  
3           latency, the branch resolution latency is the number of  
4           instruction cycles to resolve a conditional branch  
5           instruction in a processor, the processor to couple to  
6           the memory.

1           12.   The memory of claim 9, wherein  
2                    the memory array is capable of being directly  
3           addressed by a processor to randomly access storage  
4           locations therein.

1        13. The memory of claim 2, wherein  
2                the memory is a first-in first-out memory.

1        14. A method for a first-in first-out (FIFO) memory, the  
2 method comprising:  
3                storing one or more prior pop pointer values of a  
4 pop pointer;  
5                processing one or more pop requests to read data  
6 from the FIFO memory;  
7                receiving information to indicate at least one of  
8 the one or more pop requests was speculative and a state  
9 of the pop pointer of the FIFO memory should be restored;  
10 and  
11                restoring one of the one or more prior pop pointer  
12 values to the pop pointer in response to the information.

1        15. The method of claim 14, wherein  
2                the one or more prior pop pointer values of the pop  
3 pointer are stored into a pointer memory.

1        16. The method of claim 15, wherein  
2                the restoring of the one prior pop pointer value to  
3 the pop pointer includes  
4                reading the one prior pop pointer value from  
5                the pop pointer memory, and

6 loading the one prior pop pointer value into  
7 the pop pointer.

1 17. The method of claim 14, further comprising:  
2 prior to the processing of the one or more pop  
3 requests,  
4 storing data into a memory array of the FIFO  
5 memory, and  
6 incrementing a push pointer.

1 18. The method of claim 17, further comprising:  
2 reading a pop pointer value of the pop pointer and a  
3 push pointer value of the push pointer, and  
4 determining a status of the memory array in response  
5 to the pop pointer value and the push pointer value.

1 19. The method of claim 18, wherein  
2 the determining of the status of the memory array is  
3 further in response to a high threshold level and a low  
4 threshold level.

1 20. The method of claim 19, wherein  
2 the high threshold level is responsive to the lesser  
3 of a maximum branch resolution latency and the low  
4 threshold level.

1 21. The method of claim 20, wherein

2           the maximum branch resolution latency is a depth of  
3           an instruction pipeline in a processor, the processor to  
4           couple to the first-in first-out memory.

1           22. The method of claim 20, wherein  
2           the branch information includes a branch resolution  
3           latency, the branch resolution latency is the number of  
4           instruction cycles to resolve a conditional branch  
5           instruction in a processor, the processor to couple to  
6           the first-in first-out memory.

1           23. The method of claim 17, further comprising:  
2           bypassing the pop pointer and the push pointer, and  
3           directly addressing the memory array of the FIFO  
4           memory to read or write data thereto.

1           24. The method of claim 17, further comprising:  
2           loading the pop pointer with an address of the  
3           memory array to randomly read data there-from.

1           25. The method of claim 17, further comprising:  
2           loading the push pointer with an address of the  
3           memory array to randomly write data thereto.

1           26. A data signal flow coupled into a first-in first out  
2           (FIFO) memory, the data signal flow comprising:

3           branch resolution latency to determine which one of  
4 one or more prior pointer values to restore into a state  
5 of a pop pointer; and

6           a branch indicator to indicate that a conditional  
7 branch instruction was resolved to take the branch.

1       27. The data signal flow of claim 26, wherein  
2           the branch resolution latency is a number indicating  
3 how many instruction cycles were executed to resolve a  
4 conditional branch instruction in a processor, the  
5 processor to couple to the first-in first-out memory.

1       28. The data signal flow of claim 26, wherein  
2           the branch resolution latency is a number indicating  
3 a depth of an instruction pipeline in a processor, the  
4 processor to couple to the first-in first-out memory

1       29. The data signal flow of claim 26, further comprising:  
2           a delayed branch indicator to indicate a delay of a  
3 branch instruction.

1       30. The data signal flow of claim 29, wherein  
2           the delayed branch indicator indicates the delay of  
3 the branch instruction is zero.

1       31. The data signal flow of claim 26, further comprising:

2           one or more pop requests to read data from a memory  
3           array of the FIFO memory.

1           32. A processing unit including:  
2               a plurality of processors, each of the processors  
3               including an instruction pipeline to speculatively  
4               execute instructions before a conditional branch is  
5               resolved;  
6               a first plurality of branch-aware first-in first-out  
7               (FIFO) memories to pass data from one processor to the  
8               next in a first direction, each branch-aware FIFO memory  
9               of the first plurality of branch-aware FIFO memories  
10              interleaved between a pair of processors of the plurality  
11              of processors;  
12              a first input branch-aware FIFO memory coupled to a  
13              first processor of the plurality of processors to receive  
14              input data in the processing unit; and  
15              a first output FIFO memory coupled to a last  
16              processor of the plurality of processors to drive output  
17              data from the processing unit.

1           33. The processing unit of claim 32, further comprising:  
2               a second plurality of branch-aware first-in first-  
3               out (FIFO) memories to pass data from one processor to  
4               the next in a second direction, each branch-aware FIFO  
5               memory of the second plurality of branch-aware FIFO



6 memories interleaved between a pair of processors of the  
7 plurality of processors;  
8 a second input branch-aware FIFO memory coupled to a  
9 last processor of the plurality of processors to receive  
10 input data in the processing unit; and  
11 a second output FIFO memory coupled to the first  
12 processor of the plurality of processors to drive output  
13 data from the processing unit.

1 34. The processing unit of claim 32, wherein  
2 each branch-aware FIFO memory includes,  
3 a memory array to store data;  
4 a push pointer coupled to the memory array to  
5 address memory locations therein to write data;  
6 a pop pointer coupled to the memory array to  
7 address memory locations therein to read data;  
8 a pointer memory coupled to the pop pointer,  
9 the pointer memory to save one or more prior pop  
10 pointer values of the pop pointer; and  
11 control logic coupled to the pointer memory,  
12 the control logic to restore one of the one or more  
13 prior pop pointer values to the pop pointer in  
14 response to branch information received from a  
15 processor.

1 35. The processing unit of claim 33, wherein  
2 each branch-aware FIFO memory includes,

3           a memory array to store data;  
4           a push pointer coupled to the memory array to  
5 address memory locations therein to write data;  
6           a pop pointer coupled to the memory array to  
7 address memory locations therein to read data;  
8           a pointer memory coupled to the pop pointer,  
9 the pointer memory to save one or more prior pop  
10 pointer values of the pop pointer; and  
11           control logic coupled to the pointer memory,  
12 the control logic to restore one of the one or more  
13 prior pop pointer values to the pop pointer in  
14 response to branch information received from a  
15 processor.

1       36. A computer system including:  
2           an input/output device;  
3           dynamic random access memory; and  
4           a multi-processor coupled to the dynamic random  
5 access memory and the input/output device, the multi-  
6 processor including,  
7           a plurality of processors, each of the  
8 processors including an instruction pipeline to  
9 speculatively execute instructions before a  
10 conditional branch is resolved;  
11           a first plurality of branch-aware first-in  
12 first-out (FIFO) memories to pass data from one  
13 processor to the next in a first direction, each

14 branch-aware FIFO memory of the first plurality of  
15 branch-aware FIFO memories interleaved between a  
16 pair of processors of the plurality of processors;  
17 a first input branch-aware FIFO memory coupled  
18 to a first processor of the plurality of processors  
19 to receive input data in the processing unit;  
20 a first output FIFO memory coupled to a last  
21 processor of the plurality of processors to drive  
22 output data from the processing unit; and  
23 wherein each branch-aware FIFO memory includes,  
24 a memory array to store data,  
25 a push pointer coupled to the memory array  
26 to address memory locations therein to write  
27 data,  
28 a pop pointer coupled to the memory array  
29 to address memory locations therein to read  
30 data,  
31 a pointer memory coupled to the pop  
32 pointer, the pointer memory to save one or more  
33 prior pop pointer values of the pop pointer,  
34 and  
35 control logic coupled to the pointer  
36 memory, the control logic to restore one of the  
37 one or more prior pop pointer values to the pop  
38 pointer in response to branch information  
39 received from a processor.

1        37. The computer system of claim 36, wherein  
2        the multi-processor further includes,  
3            a second plurality of branch-aware first-in  
4        first-out (FIFO) memories to pass data from one  
5        processor to the next in a second direction, each  
6        branch-aware FIFO memory of the second plurality of  
7        branch-aware FIFO memories interleaved between a  
8        pair of processors of the plurality of processors;  
9            a second input branch-aware FIFO memory coupled  
10       to a last processor of the plurality of processors  
11       to receive input data in the processing unit; and  
12            a second output FIFO memory coupled to the  
13       first processor of the plurality of processors to  
14       drive output data from the processing unit.

1        38. A processor comprising:  
2            an instruction pipeline to speculatively execute  
3        instructions before a conditional branch is resolved; and  
4            a first branch-aware first-in first-out (FIFO)  
5        memory to pass data from the processor to another  
6        processor, the first branch-aware FIFO memory to receive  
7        branch information responsive to the conditional branch,  
8        the first branch-aware FIFO memory including  
9            a memory array to store data,  
10            a push pointer coupled to the memory array to  
11        address memory locations therein to write data,

12           a pop pointer coupled to the memory array to  
13           address memory locations therein to read data,  
14           a pointer memory coupled to the pop pointer,  
15           the pointer memory to save one or more prior pop  
16           pointer values of the pop pointer, and  
17           control logic coupled to the pointer memory,  
18           the control logic to restore one of the one or more  
19           prior pop pointer values to the pop pointer in  
20           response to the branch information.

1       39. The processor of claim 38, wherein  
2           the branch information includes a branch flag to  
3           indicate a condition requiring restoration of the one  
4           prior pop pointer value to the pop pointer.

1       40. The processor of claim 38, wherein  
2           the pointer memory saves a plurality of prior pop  
3           pointer values as a history of pop pointer values.

1       41. The processor of claim 38, further comprising:  
2           status logic coupled to the pop pointer and the push  
3           pointer to monitor a pop pointer value of the pop pointer  
4           and a push pointer value of the push pointer to provide  
5           an indication of an amount of data stored in the memory  
6           array.

1       42. The processor of claim 41, wherein

2           the status logic to generate a high status flag in  
3           response to an amount of data stored in the memory array  
4           being greater than or equal to a high threshold level,  
5           and less than or equal to a maximum utilization level.

1           43. The processor of claim 41, wherein  
2                 the status logic to further generate a low status  
3           flag in response to an amount of data stored in the  
4           memory array being less than or equal to a low threshold  
5           level and greater than or equal to an empty threshold  
6           level.

1           44. The processor of claim 42, wherein  
2                 the high threshold level is responsive to the lesser  
3           of a maximum branch resolution latency and a low  
4           threshold level.

1           45. The processor of claim 44, wherein  
2                 the maximum branch resolution latency is a depth of  
3           an instruction pipeline in a processor, the processor to  
4           couple to the first-in first-out memory.

1           46. The processor of claim 38, wherein  
2                 the branch information includes a branch resolution  
3           latency, the branch resolution latency is the number of  
4           instruction cycles to resolve a conditional branch

5 instruction in a processor, the processor to couple to  
6 the memory.

1 47. The processor of claim 38, wherein  
2 the memory array is capable of being directly  
3 addressed to randomly access storage locations therein.

1 48. The processor of claim 38, further comprising:  
2 a second branch-aware first-in first-out (FIFO)  
3 memory to pass data from another processor to the  
4 processor.

1 49. The processor of claim 48, wherein  
2 the second branch-aware FIFO memory to receive  
3 branch information responsive to a second conditional  
4 branch, and  
5 the second branch-aware FIFO memory includes:  
6 a second memory array to store data,  
7 a second push pointer coupled to the second  
8 memory array to address memory locations therein to  
9 write data,  
10 a second pop pointer coupled to the second  
11 memory array to address memory locations therein to  
12 read data,  
13 a second pointer memory coupled to the second  
14 pop pointer, the second pointer memory to save one

15 or more prior second pop pointer values of the  
16 second pop pointer, and  
17 a second control logic coupled to the second  
18 pointer memory, the second control logic to restore  
19 one of the one or more prior second pop pointer  
20 values to the second pop pointer in response to the  
21 second branch information.